

1 CLAIMS

1. A decoder, comprising:
 - a. a synchronous portion, disposed to receive and responsive to a clocked signal;
 - 5 b. an asynchronous portion, coupled with an asynchronous circuit; and
 - c. a feedback-resetting portion, coupled with the synchronous portion and the asynchronous portion and interposed there between, the feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion responsive to a predetermined asynchronous reset signal.
- 10 2. The decoder of Claim 1, wherein the feedback-resetting portion substantially isolates the synchronous portion from the asynchronous portion responsive to a predetermined monitor signal.
- 15 3. The decoder of Claim 1, further comprising an inverter and a plurality of buffer stages, selected ones of the plurality of buffer stages having a skew there between reducing load capacitance thereby.
- 20 4. The decoder of Claim 1, wherein the decoder is an asynchronously-resettable row decoder.
- 25 5. The decoder of Claim 1, wherein the decoder is an asynchronously-resettable column decoder.
- 30 6. A decoder in a memory module having a plurality of memory cell groups, comprising:
 - a. a signal input;
 - b. a first memory output coupled with a first memory cell group;

- 1 c. a second memory output coupled with a second memory
cell group; and
- 1 d. a selector coupled between the signal input, the first
memory output, and the second memory output,
- 5 wherein the decoder decodes the first memory cell group, and
being disposed to select and decode the second memory cell group
responsive to an group-select signal.
- 10 7. The decoder of Claim 6, wherein the selector comprises a
multiplexer, the multiplexer selecting to decode from one
of the first memory cell group and a memory second memory
cell, the multiplexer being responsive to the group-select
signal.
- 15 8. The decoder of Claim 6, wherein the decoder is a row
decoder disposed in a memory module having a plurality of
adjacent memory rows, and wherein first memory row and a
second memory row are adjacent memory rows in the memory
module, and the group-select signal is an alternative-row-
select signal.
- 20 9. The decoder of Claim 6, wherein the decoder is a column
decoder disposed in a memory module having a plurality of
adjacent memory columns, and wherein first memory column
and a second memory column are adjacent memory column in
the memory module, and the group-select signal is an
alternative-column-select signal.
- 25 10. The decoder of Claim 6, wherein the decoder is a row
decoder disposed in a memory module having assigned memory
rows and a redundant memory row, and wherein the first
memory row is an assigned memory row, the second memory row
is the redundant memory row and the group-select signal is
a redundant-row-select signal.

- 1 11. The decoder of Claim 6, wherein the decoder is a column
 decoder disposed in a memory module having assigned memory
 columns and a redundant memory column, and wherein the
 first memory row is an assigned memory column, the second
5 memory column is the redundant memory column and the group-
 select signal is a redundant-column-select signal.
- 10 12. A decoder in a memory module having a plurality of memory
 cell groups, comprising:
15 a. a synchronous portion, disposed to receive and
 responsive to a clocked signal;
 b. an asynchronous portion, coupled with an asynchronous
 circuit in a selected memory cell group;
 c. a feedback-resetting portion, coupled with the
 synchronous portion and the asynchronous portion and
 interposed there between, the feedback-resetting
 portion substantially isolating the synchronous
 portion from the asynchronous portion responsive to
 a predetermined asynchronous reset signal;
20 d. a signal input;
 e. a first memory output coupled with a first memory cell
 group;
 f. a second memory output coupled with a second memory
 cell group; and
25 g. a selector coupled between the signal input, the first
 memory output, and the second memory output, wherein
 the decoder decodes the first memory cell group, and
 being disposed to select and decode the second memory
 cell group responsive to an group-select signal.
- 30 13. The decoder of Claim 12, wherein the selector comprises a
 multiplexer, the multiplexer selecting to decode from one
 of the first memory cell group and a memory second memory
 cell, the multiplexer being responsive to the group-select
35 signal.

- 1 14. The decoder of Claim 12, wherein the decoder is a row
decoder disposed in a memory module having a plurality of
adjacent memory rows, and wherein first memory row and a
second memory row are adjacent memory rows in the memory
5 module, and the group-select signal is an alternative-row-
select signal.
- 10 15. The decoder of Claim 12, wherein the decoder is a column
decoder disposed in a memory module having a plurality of
adjacent memory columns, and wherein first memory column
and a second memory column are adjacent memory column in
the memory module, and the group-select signal is an
alternative-column-select signal.
- 15 16. The decoder of Claim 12, wherein the decoder is a row
decoder disposed in a memory module having assigned memory
rows and a redundant memory row, and wherein the first
memory row is an assigned memory row, the second memory row
is the redundant memory row and the group-select signal is
a redundant-row-select signal.
- 20 17. The decoder of Claim 12, wherein the decoder is a column
decoder disposed in a memory module having assigned memory
columns and a redundant memory column, and wherein the
first memory row is an assigned memory column, the second
memory column is the redundant memory column and the group-
select signal is a redundant-column-select signal.

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